DESIGN OF LOW POWER FULL ADDER CIRCUIT USING ADIABATIC LOGIC

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ABSTRACT:

Due to the increasing demand in mobile electronic devices, power efficient VLSI circuits are required. Computations in the devices need to be performed using low power circuits operating at greater speed. Addition is the most basic arithmetic operation and adder is the most fundamental arithmetic component of the processor. Adders are the key building blocks in arithmetic and logic units and hence increasing their speed and reducing their power consumption strongly affects the speed and power consumption of processor. Ripple carry adder achieves less area and high speed for many data processing processors to perform fast arithmetic functions. In many computational systems the delay and power consumption problem is eliminated by using low power consumption methods. Mostly CMOS technology is used to design low power digital circuits. Adiabatic logic circuits offer significant reduction in power dissipation when compared with static CMOS. Adiabatic switching logic conserves the energy instead of heat dissipation. The functionality and performance analysis is carried out using Tanner EDA tool.

Key words: Carry propagation adder, low power design.

1.INTRODUCTION

Increasing demand in mobile electronic devices, power efficient VLSI circuits are required. Computations in the devices need to be performed using low power circuits operating at greater speed.

Adders are the key building blocks in arithmetic and logic units and hence increasing their speed and reducing their power consumption strongly affects the speed and power consumption of processor. Different logic styles, each having its own merits and demerits. The designs are classified into two categories:

- static style and
- dynamic style

Static full adders are more simpler, and required less power but the chip area requirement is larger compared with its dynamic counterpart. Different logic styles tend to favor one performance aspect at the expense of others. Static (CMOS) logic, dynamic CMOS logic, complementary pass-transistor logic (CPL) and transmission

gate full adder (TGA) are the most important logic design styles in the conventional domain. The advantages of static (CMOS) logic adders (with 28 transistors) are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and requirement of buffers. Another complementary type adder is mirror adder with almost same power consumption and transistor count (as that of [3]) but the maximum carry propagation path/delay inside the adder is relatively smaller than that of the static CMOS logic. On the other hand, CPL shows good voltage swing restoration employing 32 transistors. However, CPL is not used for low-power applications. Because of its high switching activity (increased switching power), high transistor count, static inverters, and overloading of its inputs are the drawback of this approach. The prime disadvantage of CPL, that is, the voltage degradation was successfully addressed in TGA, which uses only 20 transistors for full adder implementation. Later, researchers focused on the hybrid logic style in order to improve the performance. The HPSC circuit, XOR, and XNOR functions were simultaneously

generated by pass transistor logic module and CMOS module to produce full- swing outputs of the full adder but at the cost of increased transistor count and decreased speed.
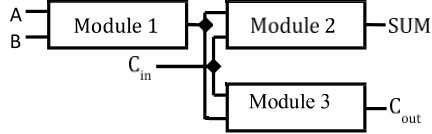
(a)

Fig.1. (a) Schematic structure of proposed full adder.

The objective of this paper is to reduce buffer count during carry propagation and optimize the different performance parameters like power, delay, and transistor count of the full adder compared with the already existing ones. The circuit was implemented using tanner EDA tool. The average power consumption (3.693μW) of the proposed circuit was reduced dramatically by deliberate incorporation of very weak CMOS inverters coupled with strong transmission gates for 1.8 V supply when implemented in tanner EDA tool. On the other hand, the layout area excluding buffer (102.94 μm2) and the delay of the circuit (205.13 ps).

2. DESIGN APPROACH OF THE PROPOSED FULL ADDER

The proposed full adder circuit is represented by three blocks as shown in Fig.a. Module 1 and module 2 are the static CMOS modules that generate the sum signal (SUM) and module 3 generates the output carry signal (Cout). Each module is designed individually such that the entire adder circuit is optimized in terms of power, delay, and area. These modules are discussed below in detail.

2.1. STATIC CMOS MODULE

In the proposed full adder circuit, static CMOS module is responsible for the power consumption of the entire circuit. Therefore, this module is designed to minimize the power to the best
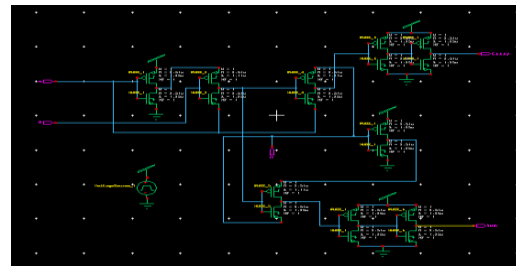

Fig.1(b) logical operation structure of proposed adder

possible extend with avoiding the voltage degradation possibility. Fig. 1(b) shows the logical operation structure of the proposed adder. Static CMOS circuit have the property of low power consumption

is implemented by weak inverter (channel width of transistors being small) formed by transistors Mp1 and Mn1 [Fig.b]. Full swing output signals is guaranteed by level restoring transistors Mp2 and Mn2 [Fig.b].

2.2. CARRY GENERATION MODULE

In the proposed circuit, the output carry signal is implemented by the transistors Mp2, Mp4, Mn2, and Mn4 as shown in Fig. 1(b). The input carry signal (Cin) propagates through a (Mn3 and Mp37).The deliberate use of strong transmission gates (channel width of transistors Mn7, Mp7, Mn8, and Mp8 is made large) guaranteed further reduction in propagation delay of the carry signal.

2.3. OPERATION OF THE PROPOSED FULL ADDER

Fig.1(b) shows the detail diagram of the proposed full adder. The sum output is granted by static CMOS logic. The inverter pair Mp1 and Mn1 generate B', which is effectively used to design the controlled inverter using the transistor pair Mp2 and Mn2. It has some voltage degradation problem, which has been removed by transistors Mp3 and Mn3. p-MOS transistors (Mp4, Mp5, and Mp6) and n-MOS transistors (Mn4, Mn5, and

Mn6) complete SUM function. Analyzing the truth table of a full adder, the condition for Cout generation has been deducted as follows:
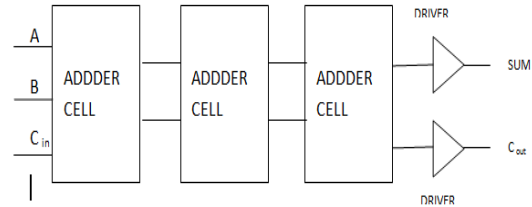
If, A = B, then Cout = B; else, Cout = Cin.

Fig. 2. Simulation test bench setup.

The parity between inputs A and B was checked, if they are same, then Cout is B, which is realized by transistors Mp3 and Mn3. Otherwise, the input carry signal (Cin) is reflected as Cout which is implemented by another pair of transistors Mp5 and Mn5.
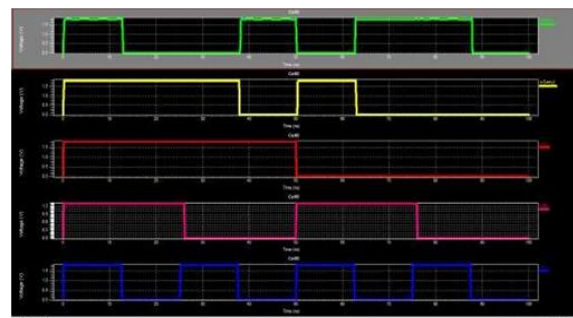

Fig.3.Output waveform of 1-bit adder

In existing method single bit adder cell was designed and it was not perform well under deployment of real- time conditions. This is because in cascaded

form, the driver adder cells may not provide proper input signal level to the next stage. It granted the faulty output of the circuit it leads to malfunction under low supply voltages. To analyze the proposed adder, a practical setup as shown in Fig. 2. To discarding of buffer in realistic environment, input buffers are removed. The inputs are directly fed logic cell. The proposed circuit is simulated using different test bench setups. These test benches are having the common type of two buffers at the output (Fig. 3). The number of stages increased gradually. It was observed that the carry propagation delay is observed from the input to output after coming stages. Therefore, 3-stage simulation test bench is used to simulate the proposed adder. Using test bench the behavior parameters are measured using second stage of the proposed circuit. This offered the tested adder cell to have the output and input capacitances of adjacent adder cells as its input and output capacitance; allowing a real time simulation environment for cascaded approach. Random signal patterns were applied at the inputs and the worst case results is accounted and compared in second stage. The proposed circuit was analyzed in tanner EDA tool at different input voltages levels.

3. ADIABATIC LOGIC AND FAMILIES

Different logic styles of adiabatic circuits have been proposed over the years and the complexity of circuits also vary according to design by number of operation clock, single - dual rail style, charging and discharging path etc. Adiabatic logic helps in the reduction of the power dissipation of the circuit. There are 2 types of adiabatic logic families:

- Fully adiabatic logic family
- Quasi adiabatic logic family

In fully adiabatic logic all charge on the load capacitance is recovered by the power supply. They have more complex structures. They dissipate less energy due to low leakage current through non ideal switches. Fully adiabatic circuits face a lot of problems with respect to the operating speed and the inputs power clock synchronization. In quasi adiabatic logic some charge is allowed to be transferred to the ground. The structures are simpler. Energy loss is directly proportional to the capacitance driven and square of threshold voltage.

3.1. PERFORMANCE ANALYSIS OF THE PROPOSED CIRCUIT

The simulation analysis was carried out in tanner EDA at varying the input voltages and compared with the other standard adder designs reported with different low power design approaches.

TABLE I SIMULATION
RESULTS FOR FULL ADDER

Design	Average power	delay	PDP	Transistor count
C-CMOS	6.2199	292.1	1.816832	28
Mirror	6.0797	281.61	1.712104	28
CPL	7.71985	183.97	1.42022	32
TFA	8.2491	287.1	2.368316	16
TGA	8.4719	293.9	2.8989	20
14 T	12.7217	381.7	4.85587	14
10 T	14.3449	132.595	1.9020602	10
HPSC	6.3798	273.7	1.74615	22
Maj bsd	6.3227	185.4	1.17222	--
24T	15.91	314.2	4.998	24
FA_hyb	5.978	252.3	1.508	24
FA_DPL	19.56	226.2	4.432	22
FA SR-CPL	20.78	220.65	4.585	20
hybrid	4.1563	224	0.931	16
propo	3.693	205.1	0.899	16
sed		3		

Discarding the buffer usage and optimization power and delay is main aim of the proposed adder circuit. the power-delay product (PDP) is minimized in the proposed case. It was observed that in the result of the design, the power consumption could be minimized by mainly using the adiabatic logic; while the carry propagation delay is improved by sizing the transistors gates present between the paths from Cin to Cout. The transistor sizes is given in Table I. Power consumption, propagation delay, and PDP of the proposed circuit along with existing circuits (from literature) are given in Tables I.

For comparison in a common environment, the proposed circuit adder and standard logics are simulated using the common test bench. The simulation was performed for varying supply voltage ranges.
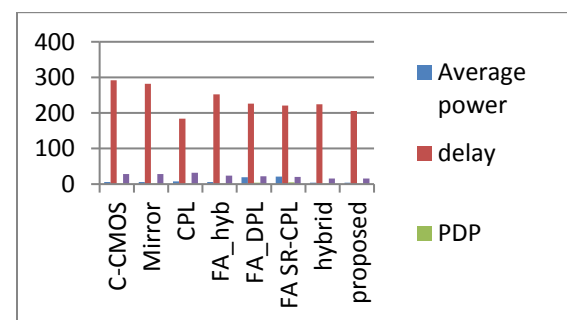
Fig.4. Comparison of PDP of various full adder designs

The majority-based adder, reported by Navi, included capacitors in their design. The proposed circuit is compared with other low power full adders reported in. The circuit of the low power full adder reported in were re-simulated in tanner EDA tool, so this paper can be authentically compared. The proposed low power adder requires only 16 transistors whereas the other low power adders require more than 20 transistors. The average power consumption is significantly lower than that of other low power adders. Less number of transistors ensuring speed of the circuit. The detailed comparison of the proposed circuit with other existing circuits are tanner EDA technology is represented in Tables I and II, respectively.

The performance of the proposed circuit in terms of power consumption and propagation delay with variation in supplied voltage was carried out (not shown here) and the corresponding comparison of the PDP (with the other existing designs) is shown in Fig. 4. The optimization of power consumption and propagation delay of the proposed circuit is explained mathematically in Sections A and B.

3.2. CALCULATION OF POWER CONSUMPTION

Power consumption is broadly classified into two categories: 1) static power and 2) dynamic and short-circuit power. Static power, arising at the levels of biasing and leakage currents, in most of the CMOS-based implementations is fairly low when compared with its dynamic counterpart. In proposed methods main aim to minimize the static power further, the weak inverters having large channel width of 800/240 nm for Mp2 and Mp4, respectively. The over- all static power in current technology was found to be 2.139 nW for 1.8-V supply which is very low when compared with the overall dynamic power (3.693μW),but the ratio (of static power: dynamic power) decreased. Decreasing static, dynamic power is achieved by semi isolating the proposed adder circuit from circumstance.

The dominant component of the power consumption, the dynamic power, arises because of charging and discharging of the load capacitances. The

load capacitance, Cload,, fixed capacitance, Cfix, and a variable capacitance, C_{var}, as follows:

$$C_{load} = C_{fix} + C_{var} \qquad (1)$$

In this, C_{fix} is the technology-dependent (principally originated from diffusion capacitance) and interconnect dependent capacitances. The interconnect dependent capacitance is minimized by efficient layout design in this case. On the other hand, C_{var} is composed of the input capacitances of subsequent stages and a part of the diffusion capacitance at the gate output and can therefore be taken care of by proper sizing of the transistors. For every low-to-high logic transition in an adder, C_{load} incurs a voltage change 0V, drawing energy (C_{load} 0V to VDD) from the supply voltage VDD. For each node j belongs to N , these transitions occur at a fraction αj of the clock frequency fc. So the total dynamic switching power can be calculated by summing over all N nodes in the circuit to N , these transitions occur at a fraction αj of the clock frequency fc. So the total dynamic switching power can be calculated by summing over all N nodes in the circuit.

Power = VDD ∗ fc ∗αj ∗ Cload j ∗ OVj

(2)

from (2) the transistor size could be an effective parameter for reducing dynamic power consumption. Subsequently, they were varied (through simulations) to obtain best performance in terms of power and delay. The optimized transistor sizes of the proposed full adder are already summarized in Table I.
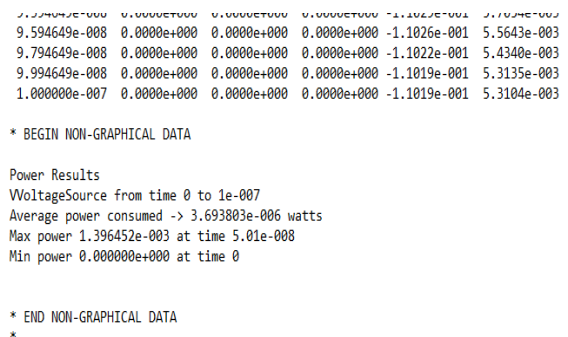


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9.594649e-008  0.0000e+000  0.0000e+000  0.0000e+000  -1.1026e-001  5.5643e-003
9.794649e-008  0.0000e+000  0.0000e+000  0.0000e+000  -1.1022e-001  5.4340e-003
9.994649e-008  0.0000e+000  0.0000e+000  0.0000e+000  -1.1019e-001  5.3135e-003
1.000000e-007  0.0000e+000  0.0000e+000  0.0000e+000  -1.1019e-001  5.3104e-003

* BEGIN NON-GRAPHICAL DATA

Power Results
VVoltageSource from time 0 to 1e-007
Average power consumed -> 3.693803e-006 watts
Max power 1.396452e-003 at time 5.01e-008
Min power 0.000000e+000 at time 0

* END NON-GRAPHICAL DATA
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Fig.5.Power Of Proposed Adder Using Adiabatic Logic

It was observed that the static power of the developed circuit varied from 56.38 to 392.4 pW for variation in supply voltage from 1.8 to 2.5 V. In contrast, the dynamic power varied from 114.08 nW to 6.125 μW for the same voltage variation. Considering the similar kind of implementation with a voltage range of 18–2.5 V, the dynamic power consumption was found to be reduced

dramatically while the static power consumption.

3.3. CALCULATION OF PROPAGATION DELAY

Because adder is the indispensable computational unit in most of the systems, its prolong predominantly governs the normal speed overall performance of the entire system. Also, the velocity of response of an adder is in the main established on the propagation prolong of the elevate signal which is typically minimized by way of decreasing path length of the carry signal. In the present design, the elevate sign is generated by two controlled transmission two of the input raise sign and either of the enter alerts A or B (when A =B). As the lift two signal propagates solely thru the single transmission gate, the raise propagation direction is minimized main to a huge discount in propagation delay. The prolong incurred in the propagation is similarly reduced through efficient transistor sizing and deliberate incorporation of Because adder is the fundamental computational unit in most of the

systems, its extend predominantly governs the usual pace performance of the entire system. Also, the pace of response of an adder is usually based on the propagation delay of the carry signal which is generally minimized by using decreasing route length of the raise signal. In the present design, the raise sign is generated with the aid of controlled transmission two of the enter lift signal and either of the enter alerts A or B (when A =B). As the carry signal propagates only thru the single transmission gate, the raise propagation route is minimized leading to a great discount in propagation delay. The prolong incurred in the propagation is similarly reduced by environment friendly transistor sizing and deliberate incorporation of strong transmission gates.
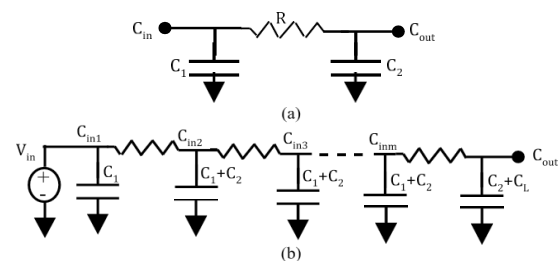

Fig..6. (a) Equivalent circuit of the for carry generation.

(b) Equivalent circuit of *m* stage-cascaded proposed full adder

The proposed circuit operating in carry propagation mode (carry propagation adder) loaded with capacitance CL can be represented by its equivalent R–C circuit as shown in Fig. 6(b).

Assuming the voltage source, Vin, to be a step waveform (for simplicity), the delay τpd(m) of the cascaded proposed full adders, can be evaluated by simplifying it into a first-order circuit having a time constant, τ , and making use of the Elmore delay approximation.

It is considered from (3) that the propagation extend of the proposed adder increases rapidly with the expand in the size of the adder chain (increases as the rectangular of m). The simulation consequences incorporating the gradual amplify in the range of levels of full two adders two also two validated this two 2nd two order two upward shove in delay with enlarge in the number of stages [Fig. 6(a)]. The simulation results [given in Fig. 6(a)] have been measured for no load capacitance and the worst case lift propagation length is represented here. Incorporation of the load capacitance extended the extend but the nature of the design remained the same. To reduce the standard delay, the buffers had been blanketed at fantastic degrees of full adder chain. For environment friendly incorporation of buffers at appropriate stages, analytical evaluation was once carried out by using extracting capacitance and resistance values from the post layout simulation results.

Considering (3) and intermediate buffer delay, the total lift propagation prolong for m, ranges after two the incorporation of intermediate buffers can be represented as

$$\tau pd(m) = 0.69[\ R(C1 + C2)\ m(m + 1)/2 + m\ R(CL - C1)] \quad (3)$$

The load capacitance, CL, of the adder chain is given in (3) is equal to the enter capacitance, C in buf, of the intermediate buffer and have been changed to derive (4). The lengthen of the buffers, tpd, buf, is unbiased of the wide variety of stages, m, and its value is received via intermediate prolong calculation which is located to be 326.26 ps.

For the proposed full adder, the Cin to Cout path ON resistances and

parasitic capacitances values extracted from postlayout simulation are as follows:

R1 = 4.2365 kK, C1 = 13.792 fF and C2 = 6.689 fF. (4)

To find the optimized number of stages, the average delay per stage (τpd(m)total)/m, value was minimized. Differentiating

this common delay fee with recognize to m, the expression for the minimal price of m is acquired as follows:

τpd(m)total = τpd(m) + τpdbuf

= 0.69[R(C1 + C2) m(m + 1)/2+ m R(CL – C1)]

= τpdbuf (5)

The minimal value of m is evaluated from (5) which turns out to be 3.26 (3).

The gorgeous quantity of two stages, m, two for achieving the minimum raiseprop agation extend is similarly authenticated by using the sensible two simulation outcomes two as proven in Fig. 6(b). From Fig. 6(b) and the mathematical result received from (5), it can be envisaged that the most optimized performance, when speed is of prime concern, is carried out using one

buffer after each and every three stages.
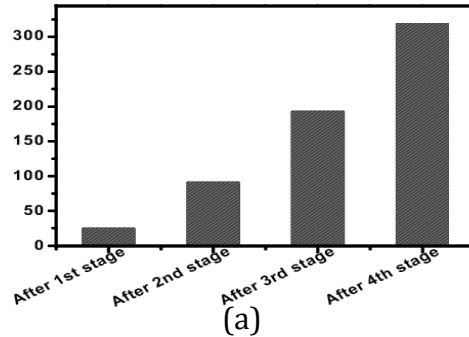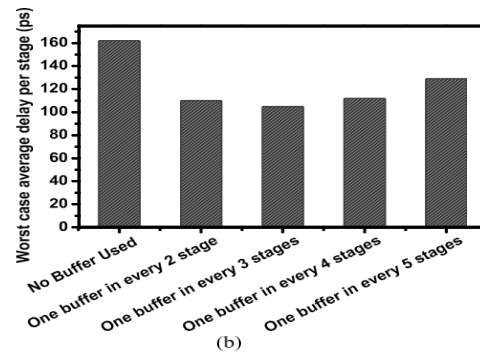
m= root of (2*τ*)/(0.69*R*(c1+c2) (6)

(a)

Fig. 7. (a) Total carry propagation delay for different stages (without load capacitance).

(b)

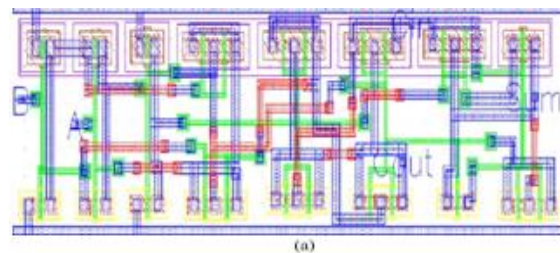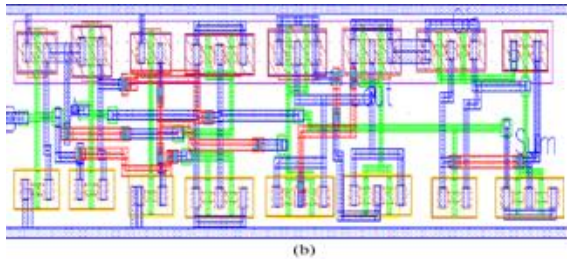(b) Variation of average delay with introduction of buffers at different stages.

Fig. 8. (a) Layout of the 1-bit full adder.

(b) Layout of the 1-bit full adder without buffer.

3.4. CALCULATION OF AREA OF 1-BIT ADDER

Fig. 8(a) and (b) shows the layout of the proposed circuit (excluding buffers). The region in of proposed circuit is 102.94 µm2. The range of transistors for the proposed circuit including buffer is 18. Hence, the region of the diagram of the proposed adder such as buffer is 218.02 µm2. With an goal to beautify the performance of the proposed full adder in terms of electricity consumption and delay,
the layout required sturdy transmission gates and vulnerable inverters. Therefore, the channel width of transistors Mp7, Mp8, Mn7, and Mn8 and transistors Mp1, Mp6, Mn1, and Mp6 (involved in inverters) (Fig.2) were made fantastically larger and smaller, respectively. The design place (excluding buffer) in the present diagram is greater (6.55%) than that of TFA which is also comprised 24 transistors. When compared with the first-rate plan in terms of region(10T), the proposed diagram of the adder (excluding buffer) consumed 44.5% greater area. But, the predominant difficulty of the proposed adder design was once minimization of PDP, which proved to be appreciably improved (51%) with appreciate to 10 T.

5. CONCLUSION

The main idea of this work is to introduce the design of high performance and power efficient RCA using adiabatic logic. The proposed method consumes low power compared to conventional method. The rapid switching of millions transistors dissipates lots of power and overheats the chip. This excessive temperature reduces the reliability of the chip and raises the need for expensive and large cooling systems. This work introduced new methodologies for low power digital design. From the output results it was found that the proposed design increases 27.70% of the power saving compared to conventional design.

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